THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte ALEXANDER D. PELEG, MILLIND MITTAL, LARRY M. MENNEMEIER, BENNY EITAN, CAROLE DULONG, EIICHI KOWASHI and WOLF WITT

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Appeal No. 1998-0524
Application No. 08/522,067

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ON BRIEF

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Before JERRY SMITH, BARRETT and HECKER, ***Administrative Patent Judges.***

HECKER, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 24 through 26 and 28 through 33, all claims pending in this application.

The invention relates generally to the field of computer systems, and in particular, the area of packed data instructions. In typical computer systems, processors are

implemented to operate on values represented by a large number of bits (e.g., 64) using instructions that produce one result. However, some applications require the manipulation of large amounts of data which may be represented in a small number of bits (e.g., in multimedia applications). To improve efficiency in such applications, certain processors provide packed data formats. A packed data format is one in which the bits typically used to represent a single value are broken into a number of fixed sized data elements, each of which represents a separate value. For example, a 64-bit register may be broken into two 32-bit elements, each of which represents a separate 32-bit value. Prior art processors provide instructions for separately manipulating each element in these packed data types in parallel. For example, a packed add instruction independently adds together corresponding data elements from a first packed data and a second packed data. Thus, if a multimedia algorithm requires a loop containing five operations that must be performed on a large number of data elements, it is desirable to pack the data and perform these operations in parallel using packed data instructions.

In this manner, these processors can more efficiently process multimedia applications.

With reference to the claimed invention, execution of a single packed data instruction causes at least two independent multiply-add operations on packed data inputs. See for example, Table 3a in Appellants' specification.

Representative independent claim 28 is reproduced as follows:

28. In a computer system, a method for manipulating a first packed data and a second packed data responsive to the execution of a single instruction, said first packed data including A_1,A_2,A_3, and A_4 as data elements, said second packed data including B_1, B_2, B_3, and B_4 as data elements, said method comprising the steps of:

multiplying together A1 [sic] and B1 [sic] to generate a first intermediate result;

multiplying together A2 [sic] and B2 [sic] to generate a second intermediate result;

multiplying together A3 [sic] and B3 [sic] to generate a third intermediate result; and

multiplying together A4 [sic] and B4 [sic] to generate a fourth intermediate result;

performing in parallel the following steps:

adding together said first intermediate result and said second intermediate result to generate a first data element in a third packed data; and

adding together said third intermediate result and said fourth intermediate result to generate a second data element in said third packed data; and

saving said third packed data for use as an operand to another instruction.

The Examiner relies on the following references:

Ando et al. 4,771,379 Sep. 13, 1988

Shipnes, “Graphics Processing with the 88110 RISC Microprocessor,” IEEE, 1992, pp. 169-174.

Claims 24 through 26 and 28 through 33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ando in view of Shipnes.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

After a careful review of the evidence before us, we will not sustain the rejection of claims 24 through 26 and 28 through 33 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan

contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995) (***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984)).

The Examiner indicates that Ando teaches the claimed invention except for explicitly disclosing the technique of performing the operations on packed data. However, since it is well known to use packed data formats to improve efficiency, as evidenced by Shipnes, the Examiner concludes that it would have been obvious to have used a packed data format in Ando to more efficiently process data, e.g., multimedia data. (Final rejection, paper no. 9 and paper no. 7.)

Appellants argue that their single instruction operation requires a multiply-add operation, **without** accumulation. The Ando-Shipnes combination **always** sums the results **of all** of the multiplications and adds **a previously stored accumulation value** to generate a **single** result value (brief-page 5).

Appellants state:

> Each of Applicant's independent claims requires either: 1) that execution of the instruction is completed **without summing/accumulating** the results of the multiply-add operations and without **adding an accumulation value** (claim 24 -"without adding said first and second data elements"; and claim 26 - "without summing said plurality of result data elements"); or
> 2) that a packed result containing the two **unaccumulated** data elements is stored as an operand for use by another instruction (claims 25 and 28). (Brief-pages 6 and 7.)

Appellants note that zeroing the accumulation value of the Ando-Shipnes combination would be costly and inefficient (brief-page 7).

The Examiner responds that **when** the accumulation value is **zero**, the Ando-Shipnes combination provides the same result. (Answer-page 5.)

We find that this explanation falls short of teaching the claimed invention. The supposition that one set of isolated circumstances would produce the same result is unconvincing. The fact that accumulation occurs at all, is contrary to the claimed invention, as argued by Appellants.

The Examiner responds further, with respect to zeroing the accumulation value:

> [S]ince the results of multiplications (e.g., A1*B1, A2*B2) of the data elements (e.g., A1, B1, A2, and B2) are for a certain period of time available in the accumulator before any addition (accumulation) can be performed, one of ordinary skill in the art, if it were considered desirable for any reason to just store the results of multiplications without adding them, would have implemented the claimed invention. (Answer-pages 5 and 6.)

We take the Examiner's response to mean that any computer programer is capable of writing a computer instruction to multiply-add, **without** accumulation, depending on the desired calculations pertaining to the algorithm being implemented. We might be convinced that such an instruction is considered to be within the skill of the typical programmer if there were some evidence of such in this record. In the absence of such evidence, we cannot support the Examiner's position.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg. v. SGS Importers Int'l***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

As pointed out above, the Examiner's rejection lacks motivation to remove the accumulator from Ando. Shipnes does not cure the deficiencies of Ando. Shipnes was merely relied upon to teach the use of the packed data format. This is not disputed by Appellants.

Thus, in view of the above, we will not sustain the Examiner's rejection of independent claims 24, 25, 26 and 28.

The remaining claims on appeal also contain the above limitations discussed in regard to the independent claims, and thereby we will not sustain the rejection as to these claims.

We have not sustained the rejection of claims 24 through 26 and 28 through 33 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

JERRY SMITH Administrative Patent Judge	)	
LEE E. BARRETT Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
STUART N. HECKER Administrative Patent Judge	)	

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